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LSI ARRAYS FOR SPACE STATIONS

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February 1976



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LSI ARRAYS FOR SPACE STATIONS

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PART I

CHARGE COUPLED DEVICES

Abstract

During this period two approaches have been taken to study CCD's and some of their fundamental limitations. First, a numerical analysis approach has been developed to solve the coupled transport and Poisson's equation for a thorough analysis of charge transfer in a CCD structure. The approach is formulated by treating the minority carriers as a surface distribution at the Si-SiO₂ interface and setting up coupled difference equations for the charge and the potential. The SOR method is proposed for solving the two dimensional Poisson's equation for the potential. Methods are suggested for handling the discontinuities to improve convergence. Second, CCD shift registers have been fabricated with parameters as suggested by Krambeck which should allow complete charge transfer independent of the transfer electrode gap width. A test instrument has been designed and constructed which can be used to test this, or any similar, three phase CCD shift register.

Introduction

In 1970 the CCD concept was introduced to the readers of Electronics magazine. An article presented there followed shortly after a paper by Amelio, Thomsett and Smith was published in the Bell System Technical Journal which announced the experimental confirmation of the charge-coupled device concept. The device concept exploits the phenomena of charge transfer along a semiconductor-insulator interface, typically Si-SiO₂ interface. A 3-phase structure is illustrated in Figure 1. The 3 electrodes, which form a one-bit cell, are sequentially pulsed with voltages forming a "traveling-wave" type of potential well. Thus one may also think about charge being placed in the traveling well and being transported by the well. Actually the well is formed in an adjacent region near the charge, and then the electric field plus diffusion forces the charge to move to this new location of the well.

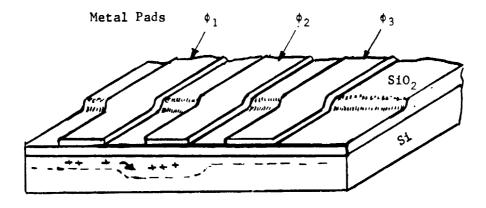


Figure 1. 3-phase CCD Structure

In Figures 2 and 3 methods are shown for gating charge into and out of the charge transfer structure. Figure 2 shows an injecting P-N junction and an insulated gate for gating charge into a shift-register type structure. Figure 3 illustrates the injection of charge by optical means. A two-dimensional scheme for charge accumulation, storage, and transfer allows the CCD to be used as a video camera. This is one of the most interesting applications of CCD's since ideally it should allow construction of a fully integrated self scanning video camera.

Charge transfer devices possess few unique functional capabilities; however, they promise ultimate simplicity for fabrication. This may lead to more extensive integration of electronic functions into single silicon chips, and it might lead to increased reliability and decreased cost.

There is a great deal of interest in CCD's for these reasons.

In the following we focus on some of the problems associated with operation of the CCD, and we discuss the theoretical and experimental approaches which we are using to study these problems.

Limitations

All electron devices have certain limitations such as finite transit times, maximum allowable currents and voltages, and maximum power gain available for stable operation. The two fundamental limitations considered here are different from those. One of the integral functions performed in the CCD is information storage, and the storage time depends upon how long the charge is in route through the charge transfer structure. Since the stored charge represents excess minority carriers, there is a finite lifetime for the excess charge. It will decay exponentially unless it is refreshed, and the lifetime represents a limitation on the memory storage time.

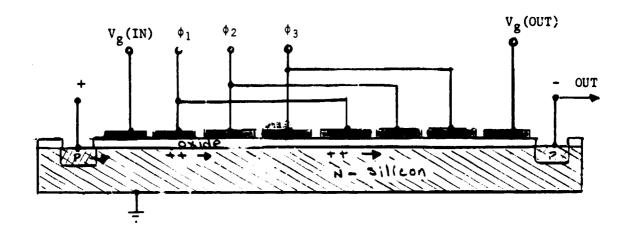


Figure 2. Use of Junctions for Input and Output Charge.

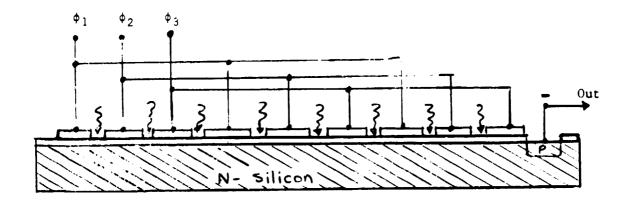


Figure 3. Image Scanner.

The second limitation is associated with the potential barrier between adjacent potential wells beneath the electrodes. When a voltage is applied to an electrode on the SiO_2 surface, it may produce a depletion region in the silicon which is on the order of 1 μ deep. One may assume that the depletion extends laterally for approximately the same distance. For complete charge transfer it is necessary that depletion regions beneath adjacent electrodes should overlap; otherwise, there will not be a complete charge transfer between the electrodes. Thus, there appears to be a restriction upon the maximum allowable spacing between the electrodes. This has been of some concern because of the limitations of fabrication technology in defining the electrode sizes and the inter-electrode gaps.

The fitent of these limitations as to storage time and maximum allowable gap spacing depends upon such things as the density and cross-section of trapping states at the $\operatorname{Si-SiO}_2$ interface and the actual interface electric potential, which in turn depends upon the fixed surface charge at the interface (Q_{SS}) and the substrate doping. We have taken two approaches to investigating these limitations. First, we have been developing analytical procedures for studying these parametric effects on charge transfer. An analysis of these effects requires the application of sophisticated techniques. In the next section the relevant theory is considered. Second, we have been involved in experimental work to construct and evaluate a CCD register which is so designed as to eliminate the barrier potential problem. This is reported in a later section.

Theory of Charge-Transport Along Si-SiO₂ Interface

The cross-section of a CCD structure is shown in Figure 4 along with a graph which gives the relative distribution of mobile charge density normal to the interface. The total charge layer consists of the "block" distribution of fixed charges and the "fillet" of mobile charge. For substrate dopings levels of $C_{\rm B} = 10^{15}~{\rm cm}^{-3}$, the total space charge layer is about one order of magnitude less than a deBye length, $L_{\rm D}$

$$L_{\rm D} = \left(\frac{kT_{\rm f}}{2g^{\alpha}n_{\star}}\right)^{\frac{1}{2}} \tag{1}$$

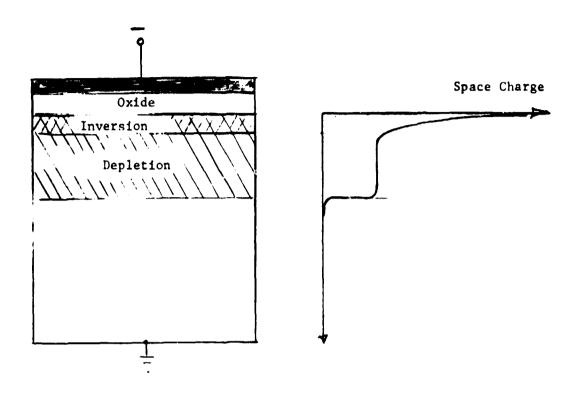


Figure 4. Charge Distribution in CCD.

For silicon at 300° K, $L_D \equiv 25~\mu$; therefore, the charge layer is approximately 2.5 μ and the "fillet" of mobile charge is considerably thinner. The fact that the mobile charge layer is thin prompts the following simplifying assumption:

The mobile charge layer can be treated as a surface sheet of charge for the purpose of transport analysis and for calculating its effect upon the potential and field distribution within the CCD. Fc. an analytical development one begins with the transport and continuity equations:

$$J_{p} = -qD_{p}\nabla P + q\mu_{p}\overline{\epsilon}P \qquad (2)$$

$$J_{n} = qD_{n}\nabla \mathbf{n} + q\mu_{n}\overline{\epsilon n}$$
 (3)

$$\frac{\partial \mathbf{p}}{\partial \mathbf{t}} = -\frac{1}{\mathbf{q}} \nabla \cdot \overline{\mathbf{J}}_{\mathbf{p}} - \mathbf{U}$$
 (4)

$$\frac{\partial \mathbf{n}}{\partial \mathbf{t}} = \frac{1}{\mathbf{q}} \nabla \cdot \overline{\mathbf{J}}_{\mathbf{n}} - \mathbf{U}$$
 (5)

We consider only currents flowing laterally along the surface when dealing with excess minority carriers, since there are no sources normal to the interface. It is necessary to deal only with the minority carrier in the surface layer. Let us assume a p-type substrate; therefore, we will analyze the transport of electrons. A surface sheet of charge, Q(x), and a surface sheet of current, I(x), are defined by:

$$O_{n}(x) = q \int_{0}^{\infty} n(x,y) dy$$
 (6)

$$I_{n}(x) = \int_{-\infty}^{\infty} J_{n}(x,y) dy$$
 (7)

Substitution into equations (3) and (5) gives:

$$I_{n}(x) = D_{n} \frac{\partial Q_{n}}{\partial x} (x,t) + \mu_{n} E_{x} Q_{n}(x,t)$$
 (8)

$$\frac{\partial Q_n}{\partial r}(x,t) = \frac{\partial I_n}{\partial x} - \dot{Q}$$
 (9)

where:

$$\hat{Q}(x) = \int_{-\infty}^{0} U(x,y) dy$$
 (10)

The quantity Q may be considered as a surface recombination rate. U(x,y) is a volume net recombination rate which could be based on the Shockley-Read or some other appropriate model. Finally the differential

equation for charge transport can be obtained by substituting (8) into (9):

$$\frac{\partial Q}{\partial t} = D_n \frac{\partial^2 Q}{\partial x^2} + \frac{\partial}{\partial x} (\mu_n E_x Q_n) - Q$$
 (11)

Equation (11) is not complete even if boundary and initial values for \mathbb{Q}_n are given because the electric field $\mathbb{E}_{\mathbf{X}}$ depends on \mathbb{Q}_n . A solution for the electric field cannot generally be obtained from a one dimensional analysis. For the CCP structure, it appears that the simplest useful form of Poisson's equation for the potential ψ (from which the field is found) is a two-dimensional problem. The general Poisson's equation is:

$$\nabla^2 \psi = -\frac{p}{E} = -\frac{q}{E} (N_d - N_a + p - n)$$
 (12)

and

$$E_{\mathbf{x}} = -\frac{\partial \psi}{\partial \mathbf{x}} . \tag{13}$$

Equation (12) can be solved with Q_n entering into the solution as a boundary condition at the interface. Both (11) and (12) must be solved simultaneously, and it seems r ther unlikely that the resultant coupled, non-linear differential equations will have a solution which can be found in a functional form. Numerical techniques can be applied directly to obtain solutions for special cases.

Figure 5 presents a diagram showing the sequence for obtaining a solution. We assume that the values of Q_n and ψ are known at time t_n ; therefore, the values for Q_n at t_{n+1} can be found by extrapolation from equation (11). With the values of Q_n at t_{n+1} , equation (12) may be solved for a new set of values for ψ . The procedure is iterated until a specified time t_N is reached.

A less complicated problem was solved by Strain and Schryer (3), and the solution is of interest because it points out certain capabilities and limitations of the CCD and indicates a possible approach to solving equation (11). They consider the case where the gap spacing between electrodes is zero. This causes the field at joints between electrodes to be infinity; however, in a numerical solution this causes no difficulty since such points are eliminated from consideration with respect to the field. The lateral field component is determined from the surface

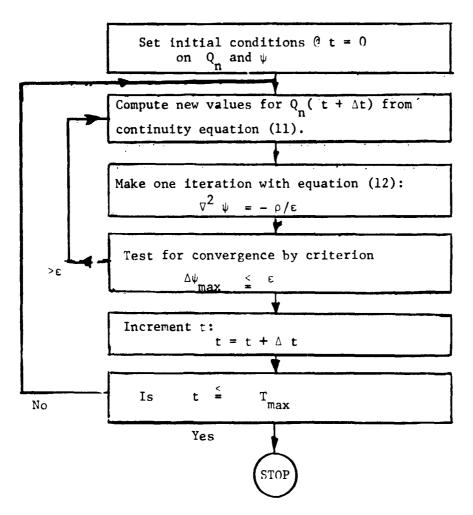


Figure 5. Flow Chart for Problem Solution.

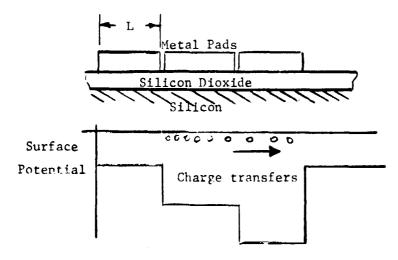


Figure 6. Structure with Zero Limit Gap Studied by Strain and Schryer.

potential, and the potential depends upon the charge on the electrodes due both to the externally applied voltage and the self-field due to the mobile charge at the interface.

The interface potential can be expressed in an approximate form as a linear function of the mobile charge at the interface:³

$$\psi(\mathbf{x}) = \psi_0 + \gamma(\mathbf{V}_{\mathbf{A}} - \mathbf{V}_{\mathbf{FB}} + \mathbf{Q}_{\mathbf{n}}/\mathbf{C}_{\mathbf{o}\mathbf{x}}) \tag{14}$$

where γ is a number between 0.7 and 1 which is chosen to make (14) give the best agreement with the exact expression for ψ . The field associated with this potential may be considered as an "external applied field."

$$E_{A} = -\frac{\partial \psi}{\partial x} = +\frac{\gamma}{C_{OX}} \frac{\partial Q_{D}}{\partial x}$$
 (15)

The "self field" is due to mutual repulsion among the charges making up the distribution Q_n . Using the method of images, Strain and Schryer show that the exact self $\frac{1}{2}$ ald can be approximated as being proportional to the derivative of Q_n , $\frac{\partial Q_n}{\partial \mathbf{x}}$.

$$E_{R} = -\frac{\delta}{\varepsilon_{OX} + \varepsilon_{S}} \frac{\partial Q_{X}}{\partial X}$$
 (16)

The total lateral interface field is $E_A + E_R$.

$$E = E_A + E_R = -\frac{\gamma \delta}{\epsilon_{OX}} + \frac{2\delta}{\epsilon_B + \epsilon_O} \frac{\partial Q_n}{\partial x}$$
 (17-A)

$$E = -S \frac{\partial Q_n}{\partial x}$$
 (17-b)

$$S = \frac{\gamma \delta}{\varepsilon_{ox}} + \frac{2\delta}{\varepsilon_{s} + \varepsilon_{ox}}$$
 (17-c)

Substitution of these results back into (11) gives

$$\frac{\partial Q_n}{\partial t} = D_n \frac{\partial^2 Q_n}{\partial x} + \mu_n Q_n \frac{\partial E_n}{\partial x} + \mu_n E_n \frac{\partial Q_n}{\partial x} - \dot{Q}$$
 (18)

Strain and Schryer also neglected the recombination at the interface so that $\dot{Q}=0$. Substitution of (17-b) have (18) gives:

$$\frac{\partial Q_n}{\partial t} = \mu S \left(\frac{\partial Q_n}{\partial t}\right)^2 + \left(D + \mu S Q_n\right) \frac{\partial^2 Q_n}{\partial x^2}$$
 (19)

Equation (19) is non-linear and one could not generally expect an analytical form of solution. With a set of initial and boundary conditions (19) can be integrated by numerical means.

The geometry considered by Strain and Schryer is shown in Figure 6. It is assumed that some initial charge distribution exists at the interface under electrode 1 and that a potential is applied to electrode 2 to attract the charge. To obtain boundary conditions, it is assumed that no current flows to the left, thus requiring $\partial Q_n/\partial x=0$ at x=0 and that the field approaches infinity in the infinitesimal gap at x=L so that $Q_n=0$ is required for a finite velocity and current. With this formulation equation (19) can be solved as a function of time on the interval $0 \le x \le L$. Strain and Schryer chose to normalize the equations and translate the zero reference for the charge. The normalizing factors are:

$$\tau = t/\tau_0$$
 , $\tau_0 = \mu u_0$ (20-a)

 $u_0 = 1 \text{ volt}$

$$y = X/L \tag{20-b}$$

$$u = SQ_n/u_0 (20-c)$$

$$a = kT/\varepsilon u_0$$
 (20-d)

$$w = u + a \tag{20-e}$$

Utilizing these normalizing factors equation (19) reduces to equation (21):

$$\frac{\partial \omega}{\partial \tau} = \left(\frac{\partial \omega}{\partial y}\right)^2 + \omega \frac{\partial^2 \omega}{\partial y^2} \quad ; \quad 0 \leq y \leq 1 \quad , \quad 0 \leq \tau \leq \infty$$
 (21-a)

$$\frac{\partial \omega}{\partial y} (0, \tau) = 0 \tag{21-b}$$

$$\omega(1,\tau) = a \qquad (21-c)$$

In order to solve (21) numerically, a suitable net or grid of points on the τ and y axes must be chosen. Thus at gridpoint (j,k) the values of y_j and τ_k are j · h and k · $\Delta \tau$ respectively. Derivatives are expressed in finite difference form:

$$\frac{\partial \omega}{\partial \tau} \triangleq \frac{\omega_{\mathbf{j}}^{\mathbf{k}+1} - \omega_{\mathbf{j}}^{\mathbf{k}}}{\Delta \tau}, \text{ or, } \frac{\omega_{\mathbf{j}}^{\mathbf{k}} - \omega_{\mathbf{j}}^{\mathbf{k}-1}}{\Delta \tau}$$

$$\frac{\partial \omega}{\partial \mathbf{y}} \triangleq \frac{\omega_{\mathbf{j}+1}^{\mathbf{k}} - \omega_{\mathbf{j}}^{\mathbf{k}}}{h}, \text{ or, } \frac{\omega_{\mathbf{j}}^{\mathbf{k}} - \omega_{\mathbf{j}-1}^{\mathbf{k}}}{h}$$

Note that there are two possible definitions, the first being called a "forward" difference and the second a "backward" difference. Presumably either formulation should give the same results; however, each must be somewhat in error because the finite difference is only an approximation. This freedom to choose the form for the finite difference allows one to choose the form optimum for the problem at hand. Strain and Schryer very cleverly chose difference forms which ultimately produced a set of linear difference equations. Their finite difference form is:

$$\frac{\omega_{j}^{k+1} - \omega_{j}^{k}}{\Delta \tau} = \frac{1}{2} \frac{\omega_{j+1}^{k+1} - \omega_{j-1}^{k+1}}{2h} \frac{\omega_{k+1}^{k} - \omega_{j-1}^{k}}{2h} + \omega_{j}^{k} \frac{\omega_{j+1}^{k} + \omega_{j-1}^{k} - 2\omega_{j}^{k}}{2} + \frac{\omega_{j+1}^{k} - \omega_{j-1}^{k}}{2h} \frac{\omega_{j+1}^{k+1} - \omega_{j-1}^{k}}{2h} + \omega_{j}^{k} \frac{\omega_{j+1}^{k+1} + \omega_{j-1}^{k+1} - 2\omega_{j}^{k+1}}{2h} + \omega_{j}^{k} \frac{\omega_{j+1}^{k+1} + \omega_{j-1}^{k+1} - 2\omega_{j}^{k+1}}{h^{2}}$$

where $1 \le j \le J$ and h = 1/J. The boundary conditions are $\omega_0^{k+1} = \omega_1^{k+1}$ and $\omega_j^{k+1} = a$.

Study of % charge remaining versus time for the zero gap limit structure.

Case A: Parabolic shaped initial distribution.

Case B: Uniformly shaped initial distribution.

$$\tau = L^2/\mu = 1$$
 nanosecond.

 $SQ_0 = 10$ volts.

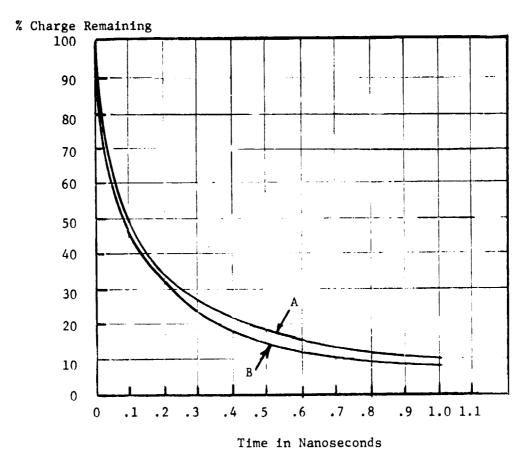


Figure 7. Plots of % Charge Remaining Versus Time.

The formulation of (22) is a generalization of the Crank-Nicholson technique which has been applied to the diffusion or heat flow equation (4). Several interesting results were obtained by numerical analysis with the digital computer. Some of these results were duplicated by us after we had written a program to solve (22). Our program is given in Appendix I. One of the results shows the charge remaining under an electrode as a function of time after the adjacent electrode is pulsed with a voltage of a polarity which attracts the excess carriers. This plot is shown in Figure 7. It reveals that the charge at first is rapidly transferred due to electric field forces and then more slowly due to diffusion forces. The actual transfer time for 100% transfer would be infinite, but practically a small fractional percent remaining may imply adequate transfer. Most applications would involve a large number of transfers in register-like structures (100 or more); therefore, a small percent loss on each transfer accumulates to a sizable loss after a number of transfers. Increasing the electrode voitages speeds up the transfer; however, the voltage must be limited to prevent breakdown or inversion in straightforward applications. Thus for a given requirement on minimum percent loss and maximum voltage, there is a minimum attainable transit time for charge transfer. Strain and Schryer also states that the transfer time is relatively independent of the initial charge distribution, and our analyses verify this. In Figure 7 the percent charge remaining vs. time is compared for several initial distributions.

As a result of their analysis Strain and Schryer predicted that CCD shift registers should be able to operate at perhaps 50 MHz bit rates. They pointed out that the "gapless" electrode structure analyzed gave unrealistic results in that most of the transfer region is "field-free." Practical gapped electrode structures produce lateral fringing fields at the Si-SiO₂ interface beneath electrodes, and these fields decrease the transfer time.

Two-Dimensional Analysis

When practical electrode structures are considered, then the fringing fields exist and must be accounted for. As pointed out previously, this requires a solution of Poisson's equation simultaneously with the transport equations. The simplest useful formulation for finding the potential is

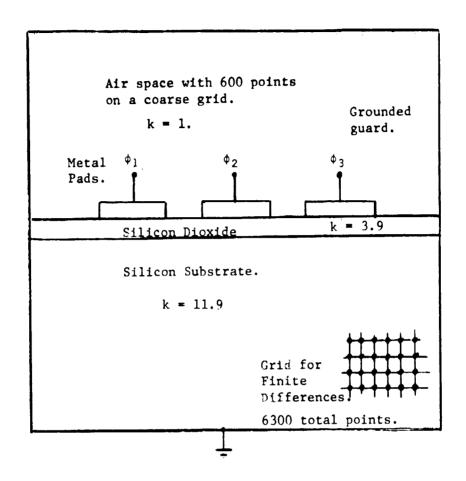


Figure 8. Geometry of the 3-electrode Problem to be Solved.

a two-dimensional model. Furthermore, one must consider a small number of electrodes to limit the size of the numerical problem to something managable with the computer. We have chosen a three-electrode structure for finding the potential, and the configuration is shown in Figure 8.

Since it is not practical to model an entire practical physical structure, one must also impose certain artificial boundaries with their attendant boundary conditions. We have done so in the following way referring to Figure 8. First, around the air space above the oxide and electrodes we have imposed a gurd or shield which has the same potential as the substrate. The substrate (silicon) is also bounded by what might

be considered to be an ohmic contact, i.e., it is assumed that the concentration is the same as the thermal equilibrium value along this boundary. Along the edge of the oxide it is either assumed that the potential is the same as that on the guard or the tangential field is zero. It is proposed that an analysis of charge transfer from electrode 1 to electrode 3 in two steps will give insight into charge transfer for a finite 3 phase shift register type of structure.

To solve for the potential we actually go back to Gauss's law rather than tackle the Poisson's equation head on. In differential form Gauss's law gives:

$$\nabla \cdot \overline{D} = \rho \tag{23}$$

where

$$\overline{D} = \varepsilon \overline{E}$$

with p the space charge density, \overline{D} the electric flux density, \overline{E} the electric field intensity and ϵ the dielectric permittivity. However, the more convenient form of Gauss's law for our purpose is the integral formulation:

$$\int_{S} \overline{D} \cdot \overline{n} ds = \int_{V} \rho dv + \int_{S} Q_{S} ds + \Sigma q i$$
 (24)

The left hand side of (24) is a surface integral over the surface enclosing the volume of interest, and \overline{n} is a unit normal vector at the point of integration. The term $\int_V \rho dv$ is a volume integral over the continuous space charge distribution. The term $\int_V Q_S ds$ represents a surface integral over all surfaces which are enclosed by the exterior surface S and which have a singular surface charge distribution Q_S . This term allows the treatment of the interface charge Q_{SS} due to oxide ions and the layer of mobile charge Q_n in the silicon. The term Σq_i is the summation of all fixed point charges within the surface S. Now any volume of interest, V, can be broken up into elementary volumes with their encompassing surfaces, most of the surfaces being mutual to two volume elements, and the integration carried out piece-wise. If the elements are small enough then the normal component of \overline{D} , i.e., $\overline{D} \cdot \overline{n}$, can be approximated in terms of a finite potential difference.

This formulation allows us to handle discontinuities in the dielectric constant and singular distributions of charge. Before going further we should note that we are taking the dimension normal to the plane of the Figure 8 to be infinite so that we can neglect contributions to the surface integrals of those ends. This allows us to actually consider only a two-dimensional geometry and is a well known technique applied to long structures such as a transmission line, etc.

We refer to Figure 9 to illustrate how that this technique can be implemented in finite differences. First of all, a grid is formed to specify a finite number of points on the bounded surface of Figure 8. The grid does not have to be uniform and in fact is chosen not to be. We can specify grid points by a dual notation (j,k) or by a single notation (I) if we specify the manner in which we count the points to arrive at (I). We assume that there are N points in a row spread across the x dimension. To get to point (I), we count from the left hand corner across to the right hand boundary, then move up one line and back to

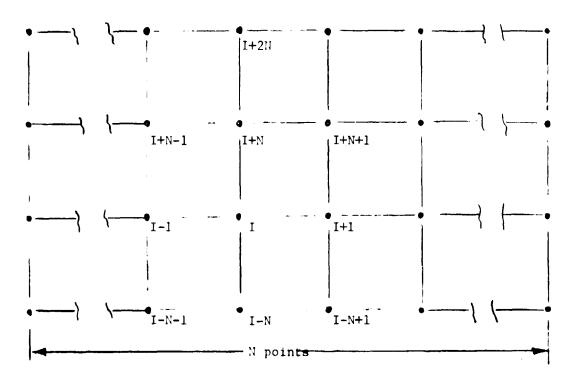


Figure 9. Grid Notation.

the left hand boundary, across again etc., until we reach the point (I). Let the point (I) correspond to (i,j). Then referring to Figure 9, points immediately surround (I) are as follows:

$$(i + 1, j)$$
 $(i + 1)$ $(i - 1, j)$ $(i - 1)$
 $(i, j + 1)$ $(i + N)$ $(i, j - 1)$ $(i - N)$

Now we apply (24) to the element of volume containing point (I) and use a finite difference approximation for $\overline{D} \cdot \overline{n}$. The left hand side of (22) for the element is:

$$\frac{1}{\varepsilon_{R}} \frac{(\psi_{I+1} - \psi_{I})}{\Delta X_{I}} \Delta Y_{I} + \frac{1}{\varepsilon_{T}} \frac{(\psi_{I+N} - \psi_{I})}{\Delta Y_{I}} \Delta X_{I}$$

$$+ \quad \overline{\epsilon}_{\mathbf{L}} \; \frac{(\psi_{\mathbf{I}-\mathbf{1}} \; - \; \psi_{\mathbf{I}})}{\Delta X_{\mathbf{I}}} \; \Delta Y_{\mathbf{I}} \; + \; \overline{\epsilon}_{\mathbf{B}} \; \frac{(\psi_{\mathbf{I}-\mathbf{N}} \; - \; \psi_{\mathbf{I}})}{\Delta X_{\mathbf{I}}} \; \Delta X_{\mathbf{I}}$$

where the notations ϵ_R , ϵ_T , ϵ_L and ϵ_B imply average values of the permittivity on the right, top, left, and bottom boundarys. The right hand side of (22) is either:

$$q(p - n + N_a - N_a)\Delta X_I \Delta Y_I$$

or, if the boundary encloses the S1-SiO₂ interface with surface charges $Q_{\rm p}$ and $Q_{\rm SS}$:

$$q(p - n + N_a - N_a) \Delta X_I \Delta Y_I + (Q_{ss} + Q_n) \Delta X_I$$

The terms p-n and Q_n depend upon the potential ψ . For the thermal equilibrium case we can use either the exponential or Fermi integral function (we have used the latter) to compute the dependence upon ψ . It is not useful to consider the surface charge Q_n if one were only interested in the thermal equilibrium case. For the transient situation one must use the coupled equations with an appropriate mode for recombination. This will be discussed later.

Now if N_T is the total number of grid points enclosed by the entire boundary, then the procedure outlined is repeated N_T times producing as many equations and unknowns. The left hand side of the equation set is linear in (ψ_T) , and the right hand side will be a nonlinear function of

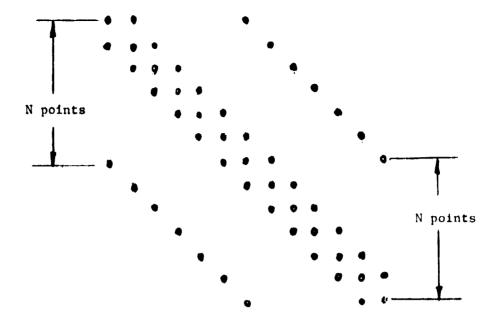


Figure 10. Form of Square Matrix on the Right Hand Side of Equation 24.

 $(\psi_{\rm I})$. The form of the matrix for the left hand side is shown in Figure 10. The matrix has a diagonal and elements on either side once removed and N-times removed. Algorithms are needed for computing $\Delta X_{\rm I}$, $\Delta Y_{\rm I}$ and the average permittivity to establish the matrix elements. This requires the use of conditional statements in the program that assign the values to the elements according to the range in which I falls. Elements of the matrix on the right hand side of (24) must also be calculated. Conditional statements are also used to limit p and n.

The first approach to solving this set of equations is a "brute force" Gauss-Seidel iterative approach. Our system to date includes $N_T=6300$ elements; therefore, straightforward Gauss elimination is impractical. We have another serious difficulty in that the system of equations is non-linear and the right-hand side depends upon (ψ_1) which is being solved for. This very likely will slow the convergence of the iterative procedure since the right-hand side is continually being readjusted. The Gauss-Seidel formulation proceeds as follows: 5

$$[A] [b] = [f] \tag{25}$$

Where [A] is the matrix of form shown in Figure 9, [+] is the column

matrix of potential values, and [f] is a column matrix with elements $f_{\rm I}$ depending on $\psi_{\rm I}$. The matrix [A] can be broken up into three parts; [D], the diagonal; [L], the lower triangular; and [U], the upper triangular.

$$[A] = [D] + [L] + [U]$$
 (26)

Therefore (26) can be written:

$$[D + L][\psi] = [-U][\psi] + [f]$$
 (27)

or

$$[\psi] = [D+L]^{-1}[-U][\psi] + [D+L]^{-1}[f]$$
 (28)

The inverse $[D+L]^{-1}$ is easier to find than the inverse $[A]^{-1}$. The iterative procedure starts with a current approximation for $[\Psi]$ called $[\Psi]^{(n)}$. Then the left hand side of (28) is taken as the next estimate $[\Psi]^{(n+1)}$. Therefore, the iterative procedure proceeds as:

$$[\psi]^{(n+1)} = [D + L]^{-1} [-U] [\psi]^{(n)} + [D + L]^{-1} [f]^{(n)}$$
 (29)

The iteration continues until $[\psi]^{n+1}$ converges to within the tolerable deviation from $[\psi]^n$. Equation (29) gives the elements of $[\psi]$ as:

$$\psi_{I}^{(n+1)} = -\frac{1}{a_{II}} \sum_{J=1}^{I-1} a_{IJ} \psi_{J}^{(n+1)} - \frac{1}{a_{II}} \sum_{J=I+1}^{N_{T}} a_{IJ} \psi_{J}^{(n)} + \frac{f_{I}}{k_{I}}$$
(30)

All elements on the right-hand side of (30) are known when $\psi_{I}^{(n+1)}$ is to be calculated.

In order to speed the convergence, the accelerated Gauss-Seidel, or successive over-relaxation (SOR), technique may be used. This procedure utilizes the results obtained from the steps outlined above. The iteration proceeds according to equation (31):

$$\psi_{\rm I}^{(n+1)} = \psi_{\rm I}^{(n)} + \omega[\langle \psi_{\rm I} \rangle^{(n+1)} - \psi_{\rm I}^{(n)}]$$
 (31)

where $<\psi_{\rm I}^{>}$ is the calculated result from equation (30). ω is called the acceleration parameter and ω < 1 corresponds to an "under-relaxation," ω = 1 corresponds to the standard Gauss-Seidel, while ω > 1 corresponds to "over-relaxation."

We have now sketched the method used for finding the potential. In Appendix II a computer program is given which has been developed to find the potential distribution when the electrode potentials, the bulk charge density, and the interface surface charge density are specified. This is the essential two-dimensional problem. Of course the desired result is the surface charge distribution of mobile charges at the Si-SiO₂ interface. In the next section we outline the method for simultaneously finding the distribution of charge simultaneously with the solution for the potential.

Solution for the Charge Distribution

The program presented in Appendix II is written to handle charge distributions in the bulk for thermal equilibrium conditions. Of course we are interested in cases where thermal equilibrium does not exist. We need a procedure for dealing with these cases as well. Our first assumption is one which is standard for most MOS calculations; namely, that the minority carrier charge density in the substrate can be neglected. All minority carrier charge will be handled as a surface charge layer at the interface. The majority carrier c entration in the substrate will be assumed to be the value at thermal equilibrium for the particular potential which exists. Since the majority carriers can move freely in the substrate in a direction normal to the interface, this seems to be a reasonable assumption that they can be depleted or accumulated as rapidly as the field changes. Minority carriers, on the other hand, must either be generated (thermally or optically) locally or transported laterally along the substrate from some source. The thermal generation mechanism is too slow to be significant during a charge transport transit time. Therefore, only those thermally generated carriers accumulated prior to the charge transfer transient are to be considered. The problem then is divided into wo parts. First the thermal equilibrium surface charge distribution prior to the transfer transient is found. Then the source of excess carriers is introduced, and the charge transfer potentials are applied to the electrodes. The transient problem is then solved.

The first step requires some model for finding the pretransient equilibrium value. We use the approach traditionally applied for analysis of the MOS structure. We assume that the interface potential for thermal

equilibrium, ψ_{80} , never exceeds in magnitude the value for strong inversion. For a P-substrate:

$$\psi_{ao} = 2 \frac{kT}{q} \ln (N_a/n_1) \qquad (32)$$

Now we introduce into (10) for the recombination rate a negative quantity, or generation rate, which will be zero if the surface potential is less than or equal to $\psi_{\rm EQ}$. A suitable function is of the form:

$$\dot{Q} = \frac{C_{c}(\psi_{so} - \psi_{s})}{\tau}$$

$$\psi_{s} > \psi_{sc}$$

$$\psi_{s} \leq \psi_{so}$$
(33)

When the transport and Poisson's equations are integrated to equilibrium from any initial condition, the surface charge Q_n will build up until ψ_s is no greater than ψ_s . After this \dot{Q} can be set equal to zero for the remaining transient solution. The parameter C_0 is a capacitance per unit area, and might be chosen as the oxide capacitance. The parameter τ is a time constant suitably chosen to expedite the solution for the initial equilibrium prior to the transfer transient.

Our first approach is to integrate the transport equation explicitly. We drop the subscript n on Q to simplify notation. We use the subscript m to count grid points from the left hand edge of the interface, i. e., $x = m\Delta x$, and we use the superscript ℓ for the time index, i.e., $t = \ell \Delta t$. Equation (11) is expressed in finite difference form:

$$\frac{Q_{m}^{\ell+1} - Q_{m}^{\ell}}{\Delta t} = D_{n} \frac{(Q_{m+1}^{\ell} - 2Q_{m}^{\ell} + Q_{m-1}^{\ell})}{\Delta x^{2}} + \frac{\mu[(\psi_{m+1}^{\ell} - \psi_{m}^{\ell})Q_{m}^{\ell} - (\psi_{m}^{\ell} - \psi_{m-1}^{\ell})Q_{m-1}^{\ell}]}{\Delta x^{2}} - \hat{Q}_{m}^{\ell} .$$
(34)

The term Q_m^{k+1} can be found from the prior values for $Q_{m+1}^{\hat{k}}$, $\gamma_m^{\hat{k}}$, ..., etc.

Note that the values of ψ along the interface are chosen from the array of values ψ_I obtained in solving the Poisson's equation. Let m=0 correspond to the value I=NL, then:

$$\psi_{\rm m} = \psi (\rm NL + m)$$

The procedure for integration of the equations can now be summarized. We start with an initial set of electrode potentials and an initial charge distribution. Poisson's equation is solved for the potential distribution using a method such as Gauss-Seidel or SOR. The required values of ψ are substituted into (34) and a new distribution for the mobile surface charge Q is obtained at a later time $t+\Delta t$ The new values of Q are substituted into the charge distribution in Poisson's equation and a new set of potentials are found.

Summary of Theoretical Work to Date

In starting this work we felt it would be helpful to become very familiar with some approach which had been successful. Therefore we programmed the solution technique outlined by Strain and Schryer and duplicated some of their results. We had hoped to be able to avoid solving Poisson's equation for gapped electrode structures; however, unjustifiable assumptions were required in order to circumvent this problem. We then began an investigation of numerical techniques for solving a two-dimensional Poisson's equation, and we have attempted to obtain thermal equilibrium type solutions. The Gauss-Seidel and SOR methods do not provide satisfactory rates of convergence so far. We believe that the situation can be improved. First, we have not tried to construct an initial solution using the method for treating the charge distribution explained in the preceding section, and this possibly will improve convergence by precluding rapid changes in the charge distribution at the interface leading to overshooting and oscillation. Second, at the expense of some complexity in programming, we can introduce the discontinuities presented by the different dielectric constants in the three media gradually. These two procedures have high potential for improving the rate of convergence. Third, we are investigating a routine for solving Poisson's equation developed at the National Center for Atmospheric Research. This program which has been used quite successfully here at MSU reportedly is much faster than the SOR method. It could at least he used to rapidly obtain initial potential estimates before applying the first and second procedures above.

Development of Test Circuitry

Our first approach to devising test circuitry for CCD registers was to design circuits to realize the ideal waveforms for the transfer electrodes on a 3-phase CCD as presented by Boyle and Smith in a review article (6). This would simplify the comparison of theoretical and experimental results in that computer programming would be simplified. Such a scheme requires the control of 3 voltage levels stepwise on the electrodes. Conceptually this procedure was very simple to design using a ring counter, simple logic, and some summing circuits and drivers. The circuits were designed and constructed with student help. However, there was an essential difficulty in obtaining the waveforms at high speeds. Finally it was decided that two level waveforms which would be more practical in application should be used. With some additional programming complexity we can simulate transfer using actual two-level waveforms easier than we can produce the actual three level waveforms.

In Figure 11 the two-level waveforms are illustrated for the transfer electrodes. Charge-transfer occurs as the waveforms on adjacent electrodes rise or fall. The system uses a three-phase clock which has an output pulse on each phase with unequal rise and fall times. The clock is a multivibrator which clocks a ring counter. The three outputs from the ring counter drive the pulse amplifiers which have unequal rise and fall times and have the capability for level adjustment. The control gate 5. the register under test is pulsed by an input sequence controller. The sequence controller is a register which can be loaded with "ones" and "zeros" in the desired pattern. The register is then clocked by the system clock either continuously or for one cycle of the register. The output of the CCD register under test can be observed with an oscilloscope for continuous operation. Operation on a one-cycle basis is monitored by an output comparison register in which the output is decoded. For this mode of operation, one loads the input register with a BCD number. The number is loaded into the register, and on push button operation it is cycled through the CCD. The output register then displays the number actually coming from the CCD register output. This feature will not be of great use a tre initial work, but the system should serve as the basis for the design of a "universal" tester for CCD registers. The block

diagram of the system is shown in Figure 12. We will later supply full details on the circuit design and operation of this tester which is the basis of a Master's thesis for a graduate student at MSU in Electrical Engineering.

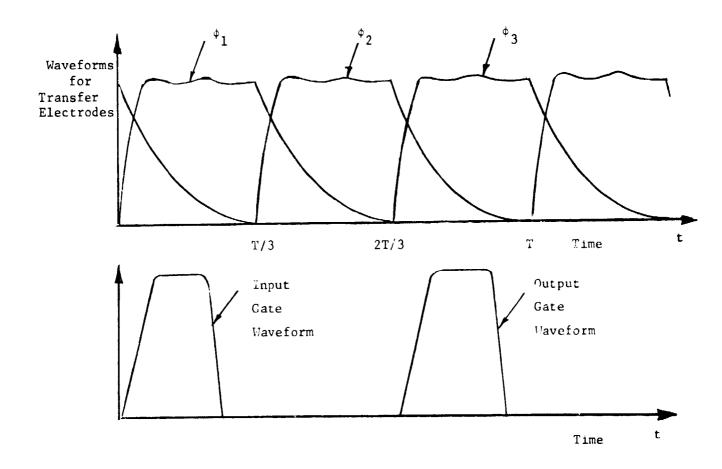


Figure 11. Waveforms for CCD test circuitry.

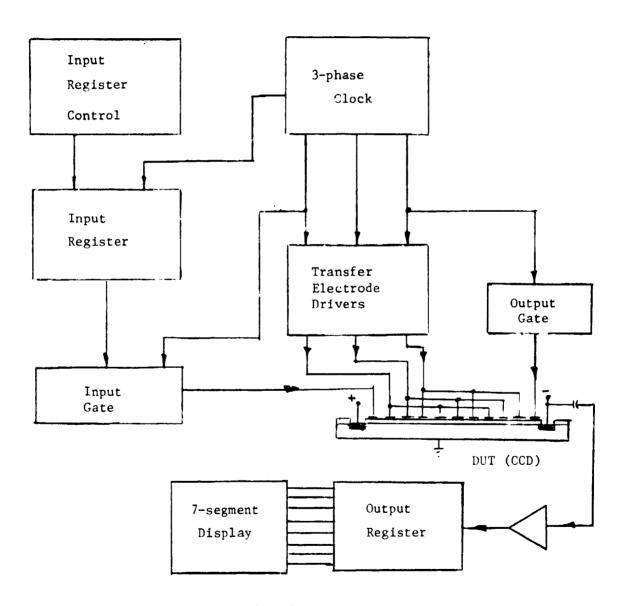


Figure 12. Block Diagram for the CCD test system.

Design and Fabrication of a CCD Register

One of the problems of CCD's discussed earlier is the potential barrier which may occur when finite gaps exist between electrodes. Earlier N-substrate devices which used holes as the mobile charge required very narrow gaps, on the order of a micron. This taxes the technology for photolithography which generally is available. Krambeck (7) showed that it was possible to choose the substrate background doping, oxide thickness, etc., in such a way that the barrier is prevented and complete charge is transferred. We refer to the article for a detailed analysis by Krambeck. Krambeck showed that complete charge would be insured if the inequality (35) on $Q_{\rm SS}$ was met:

$$\sqrt{2N\epsilon_{s}V_{2}q} + \frac{\epsilon_{ox}}{\delta}(V_{2} - V_{1}) \leq Q_{ss} \leq \sqrt{2N\epsilon_{s}V_{1}q}$$

where N is the background doping, V_2 and V_1 are potentials on adjacent electrodes, δ is the oxide thickness and ϵ and q are the permittivity and electronic charge. From this result Krambeck concluded that the a p-substrate with a doping of 10^{15} cm⁻³ or less and a good quality oxide would allow complete transfer independent of the electrode gap spacing.

Our experimental work here consisted of fabricating and packing 16 CCD shift register, each with 16 bits, test devices. We used both <111> and <100> silicon. For the geometry we consulted with Mr. Ben Hollis and settled on a 0.3 mil gap spacing and 0.6 mil pad width which was considered to be feasible with the photolithographic capabilities at MSFC. Using this criterion the metallization appeared to be good on the majority of the devices made.

The <111> silicon gave flat band voltages from -2.5 to -3 volts with approximately 1000 angstroms of oxide on a substrate with 3.8 x 10^{15} cm⁻³ doping. The minimum $Q_{\rm SS}/q$ was approximately 4.8 x 10^{11} cm⁻² for the surface state charge. From Kranbeck's curves in Figure (3) (reference 7), this material when so processed falls in the midrange for maximum and minimum values. The <100> material gave flatband values of -1.3 v to -1.6 v depending on the annealing process used after oxidation. All oxides were grown in dry O_2 at 1150°C and were annealed in N_2 at 1150°C for times from zero to 20 minutes. The $Q_{\rm SS}/q$ values are approximately 2 x 10^{11} cm⁻²

which are also in range but near the minimum values on Krambeck's chart. Higher values of $Q_{\rm SS}/q$ could have been obtained by eliminating the sintering step after metallization; however, from experience it was anticipated by Mr. Hollis that the bonding pads would pull away from the substrate if the sintering step were deleted. The remainder of the process followed the P-channel MOS procedures at MSFC with the exception of the predeposition, second oxidation, and the gate oxidation:

- 3-2 Predeposition
 - (a) 980°C furnace.
 - (b) 8.8 ssb $N_2 + 4.4$ ssb O_2 , 5 minutes.
 - (c) Add 12 ssb, 1% PH, in Argon for 7.5 minutes.
 - (d) Remove PH_3 , continue $N_2:0_2$ for 5 minutes.
- 3-3 Phosphorous glass removal
 - (a) 15-30 second 10:1 HF dip, room temperature.
 - (b) 10 minute soak in D.I. H₂O.
 - (c) Blow dry with N₂.
- 4. Second Oxidation (Dry out and drive-in)
 - (a) 1150°C furnace.
 - (b) $10 \text{ gb } 0_2 \text{ for } 10 \text{ minutes.}$
 - (c) 10 gb N₂ for 5 minutes.
- 5. Channel Photoresist
- 5-5 Etch with buffered oxide etch at 50°C for approximately 3 minutes.
- 6. Channel Oxidation
- 6-1 Same
- 6-2 Oxidation
 - (a) 1150°C furnace
 - (b) Water warmup, 1 minute, 10 gb N₂.
 - (c) Oxidize, 30 minute, 10 gb 0_2 .
 - (d) Anneal, 0-10-20 minutes, 10 gb N_2 .

The predeposition gave a 30 ohm N-type layer. After subsequent drivein and channel oxidation the layer had approximately 21 ohms resistance and junctions had approximately 35 volt breakdown. Flow rates were measured on Matheson meters except for the predep step which used the Brooks meters on the CMOS doping system.

Concurrent with fabrication of the CCD register MOS transistors and capacitors were fabricated on test wafers. Flat band threshold and

breakdown voltages were obtained from these test devices. Channel oxide thicknesses were approximately 1100 Å on test wafers. All transistors were depletion mode with the exception of the <100> devices with 20 minute anneal which had a flatband voltage of -1.3 v and a threshold of + .8 v. These devices would probably fall below the minimum on Krambeck's curves.

A photograph of the resultant CCD structure is shown in Figure 13. Note that the transfer electrodes for two phases can be connected and brought out to bonding pads all on top of the oxide. The transfer electrodes on phase one are interconnected by N tunnels. This could conceivably cause a problem which will be discussed later. The entire fabrication required only 4 mask levels. The mask design was done using the computer controlled graphics facility in the technology division.

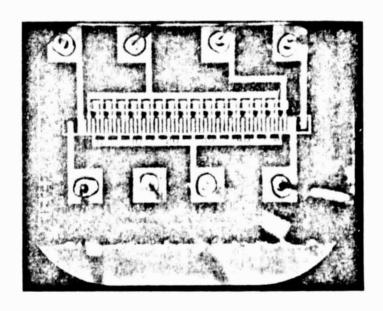


Figure 13. Photograph of Packaged CCD's.

Device Evaluation

So far only preliminary checks have been made. We expect to be evaluating the charge transfer capability during the next two months. Preliminary checks indicate that the channel is inverted with no electrode voltage. This might be inferred from the fact that $Q_{\rm SS}$ falls within Kranbeck's allowable range. Consequently there is leakage between all junctions. For example on <111> devices the leakage between the collector and substrate is $50-80\mu A$, from source to substrate $120-150\mu A$, and from phase 1 to substrate $200\mu A$.

It seems clear that there will be a conductive current between the source and collector which will be modulated to some extent independent of the control gate action. This poses a problem concerning detection, because there will be a current pulse whether excess carriers are injected or not. Only an experimental investigation will determine how serious this problem is. We anticipate that the conductive coupling from phase 1 to the collector will be strong enough to cause a significant output. However, this coupling will occur as phase 3 finishes; therefore, strobing to read during a fraction of phase 3 could remedy this. The problem can be eliminated by connections over the oxide using a silicon gate technique or by double diffusions to form the cross-unders. The decision to use the singly diffused tunnels was made when it was clear that the silicon-gate technique could not be worked out in the available time. The feasibility of the technique for wide gapped CCD structures should be apparent from testing these devices. Effects which result from non-optimum construction can be circumvented.

Acknowledgements

The help of Mr. Ben Hollis of MSFC in carrying out the entire fabrication is acknowledged. Others who helped greatly were Dr. D. Woo (Sperry) and Mr. Don Routh (MSFC) with mask design and fabrication; Mr. Bill Dow (MSFC), Mr. Tony Margarella (MSFC), Mr. Sid Ostis (Sperry), Mr. Grady Smith (MSFC), Mr. Roy Hunt (MSFC) with fabrication and evaluation procedures. Mr. Bobby Kennedy (MSFC) cooperated in making facilities available. Mr. D.L. Anderson and Mr. Al Bailey were helpful with encouragement and discussions on the project. Thanks are due to all these people and to Mr. J. Taylor for making it possible to carry out this work within the Technology Division.

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PART II

IMPURITY DIFFUSION

Abstract

We first studied the application of previously developed models to the case of a boron-nitride source. It was found that the predeposition program presented in the last report could be used to model the predeposition from such a source. The program was modified to include a temperature dependent solid solubility, and the calculated sheet resistances agreed well with experimental values for temperatures in excess of 950°C. Below 950°C, the error in calculated and measured values increase with decreasing temperature. After some study it was concluded that the discrepancy is at least in part due to inaccuracies in the measurement of high resistance layers.

Most diffusions involving spin-on liquid type sources essentially utilize a doped oxide source. To handle these type sources as well as diffusion from pyrolytically deposited doped oxides, the work of Barry and Olofsen was incorporated into the previous program to handle the predep phase of the diffusion.

Introduction

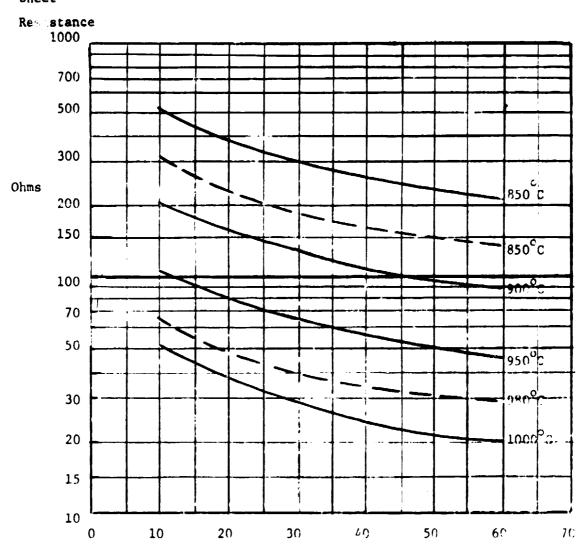
In the last report two programs were included which were of use for estimating the properties of diffused layers for various ambient sequences. One of these programs used the implicit method for solving the difference equations for diffusion and incorporated the effect of the "built-in" field which aids diffusion at high impurity concentrations and low temperature. This program was successful in simulating predepositions using a diborane source and also for simulating complex drive-in processes such as used in practical conditions for device simulation. The objective was to find suitable modifications of the program which would make it useful for simulating diffusions from boron-nitride and doped oxide sources. The work done toward these ends is reported in the following.

Boron-Nitride

The boron-nitride diffusion utilizes a source in which silicon wafers are placed vertically between boron-nitride wafers. Before diffusion is done the boat is put into a furnace with an 0_2 ambient which oxidizes the boron nitride wafers. The wafer surface is converted to 0_2 03. When the boat is further loaded with silicon wafers and placed in a furnace with a nitrogen ambient, but including a small 0_2 content, the 0_2 03 decomposes and particles of 0_2 03 are deposited on the silicon. A thin layer of glass presumed to be a mixture of 0_2 03 and 0_2 04, is formed on the silicon surface. It may be used as a source or etched away with a 0_2 1 HF etch, which rapidly etches the glass, and the impurity layer obtained in the silicon as the glass was deposited can be used as a source. The first estimate of a process model is based on the assumption that the source maintains the surface concentration at the solid solubility limit during the predeposition. If this is true, then one concludes that the predep gives the same type of profile as obtained with a diborane source.

The above hypothesis was tested with the program and some results are given in Figure 1. These curves are those given by Goldsmith, et. al. which are measured values of sheet resistance vs. diffusion time for constant temperature. Superposed are some curves calculated with the previously described computer program. It is assumed that the surface concentration is that corresponding to the solid solubility limit at the





Predeposition time in minutes

Figure 1. Sheet resistance versus predeposition time for a Boron Nitride source.

Solid curves are measured values obtained

from data by Carborundum Corporation.

Dashed curves computed with program.

diffusion temperature. The calculated results agree very well down to 950°C, and then they are progressively in error.

Our first reaction to this result was to seek for physical explanations for the model error and for methods, perhaps empirical, for describing the time-temperature dependence of the curves. After attempting to measure layers with high sheet resistance and talking with others who had experience, we found that measurements of high resistance layers are imprecise. Usually the light doping results in non-ohmic type contacts so that the measurements are polarity sensitive. An average of measurements is usually taken which is not the true sheet resistance. Therefore, we concluded that our program may not be in as much error as it apparently is at low temperature. What we plan to do now is to test our ability to predict sheet resistance and junction depth after a drive-in is accomplished. If our results are good then we can use our previous programs to generate data for boron nitride diffusions.

Doped Oxide Sources

There has been a great deal of interest in the use of doped oxides as diffusion sources because profiles can be produced without ever introducing heavy surface concentrations which strain the lattice. Doped oxides can be prepared as surface layer sources by at least two methods. First the doped oxide may be produced by a pyrolytic technique. Second, liquid sources with a suspension of doped oxide particles can be applied with a spinner. The liquid carrier is volatile and evaporates leaving a layer of particles. The layer is soft and can be wiped off, but after a low temperature (200°C) heat treatment the layer is densified. The resultant layer can be scraped from the wafer with a sharp instrument but will not be removed by ordinary contacts. Both the pyrolytic and "spin-on" oxides are less dense than a thermal oxide.

Barry and Olofsen² studied diffusion from a doped oxide and gave an approximate analytical expression for the resultant profile. Their equation is:

$$C(x,t) = C_s \operatorname{erf} \left(\frac{x}{2\sqrt{D_2 t}} \right)$$

$$C_s = \frac{mC_0 \sqrt{D_1/D_2}}{m + \sqrt{D_1/D_2}}$$
(1)

where: D_1,D_2 -- diffusivities in oxide and silicon respectively.

Co -- impurity concentration in the oxide.

m -- the segregation coefficient

We have had a report³ that Barry and Olofsen's formula describes the actual experimental results well. Our original program was modified to include equation (1) to describe the predeposition profile. Subsequent diffusion and oxidation is modeled by the program just as for other type predepositions.

We believe that the modified programs can be used to generate good predictions of diffused layer properties and plan to obtain numerical data during the next period of work.

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PART III

TRENDS IN SOLID STATE ELECTRONICS

Abstract

A selected bibliography of sources supplied in the quarterly reports and obtained in the fourth quarter is presented. The material is arranged as follows: (1) CCD's, (2) Bubble Domain Devices, (3) Amorphous Semiconductors, (4) Ion Implantation, (5) Fabrication. Each section is briefly summarized.

Trends in CCDs

Work continues on the two major problems encountered in the simply constructed CCD: (1) loss of charge due to trapping at the Si-SiO₂ interface (2) loss of charge due to potential barriers 8n inter-electrode regions.

Walden et al¹ have investigated the use of a buried layer. Here a thin P-layer is diffused or ion implanted under the channel oxide on an N-substrate. The collector is biased to deplete this P-layer. Excess charge is then injected and transferred along the P-N junction which has a lower effective trap density than exists at the Si-SiO₂ interface. These devices did not work satisfactorily; however, it was reported that Fair-child had fabricated a successful shift register using this technique.²

The approach to the gap problem previously was to use overlapping electrodes fabricated with a more complex technology; i.e.. using silicon gate techniques. Krambeck³ proposed the use of P-substrates and controlled $Q_{\rm SS}$ to obtain a surface on which potential barriers in the interelectrode region will not form. The title of a recent paper on "conductively coupled CCDs" at the International Electron Device Conference indicates this work may have been carried further.

There has also been much interest in simplifying the electrical drive requirements for the CCD. Krambeck, et al. 4 fabricated a two-phase CCD with the necessary asymmetry obtained by boron ion implants on one side of each transfer electrode. The substrate is P type and the negatively charged implants repel electrons. With equal potentials on both phases the carriers will bunch at one electrode edge ready to transfer to the

next electrode as it goes more positive. They claimed very good results. Melen and Meindl⁵ used a previously proposed technique utilizing two oxide thickness to obtain a single phase CCD. Actually one set of electrodes has a fixed bias. The drive requirements appear to be simple and practical.

The theoretical study of charge transport continues to be of interest.

Carnes, et. al.⁶, McKenna and Schryer, Strain, and Lee and Heller have published analyses and results for charge transfer efficiency. Amelio published extensive results from a numerical analysis of the CCD structure. His results supported Krambeck's prediction that potential barriers could be eliminated on P-substrates.

Perhaps the biggest news of 1972 on CCD's was Bell's announcement of the CCD self-scanning camera. Images obtained with the camera were shown at the 1972 IEEE convention in New York. An article subsequently appeared in Electronics in March. 11

Thomsett¹² demonstrated a simple charge regenerator technique to cope with the trapping problem in CCD's by refreshing the charge before it is too weak to detect.

- 1. R. H. Walden, Et. al., "The Buried Channel Charge Coupled Device," BSTJ, Vol. 51, No. 7, Sept. 1972, p. 1635.
- 2. "Buried Channels Point the Way to Solid-State Imager," Electronics, Vol. 45, No. 10, 1972, p. 29-30.
- 3. R. Krambeck, "Zero Loss Transfer Across Gaps in a CCD," BSTJ, Vol. 50, No. 10, Dec. 1971, p. 3169-3175.
- 4. R. Krambeck, et al., "A Doped Surface Two-Phase CCD," BSTJ, Vol. 51, No. 8, Oct. 1972, p. 1849-1866.
- 5. R. D. Melen and J. D. Meindl, One-Phase CCD--A New Approach to CCD Clocking," IEEE Jour. Solid State Circuits, Vol. SC-7-No. 1, Feb 1972, p. 92.

- 6. J. E. Carnes, et. al., "Free Charge Transfer in CCDs", IEEE Trans. ED. ED-19. No. 6, June 1972, p. 798-808.
- 7. J. McKenna and N. L. Schryer, "On the Accuracy of the Depletion Layer Approximation for CCDs," BSTJ, Vol. 51, No. 7, Sept. 1972, p. 1471.
- 8. R. J. Strain, "Properties of an Idealized Traveling-Wave Charge-Coupled Device," IEEE Trans. ED, ED-19, No. 10, October 1972, p. 1119.
- 9. H. S. Lee and L. G. Heller, "Charge-Coupled Method of Charge-Coupled-Device Analysis," IEEE Trans. ED, ED-19, No. 12, Dec. 1972, p. 1270-1279.
- 10. G. F. Amelio, "Computer Modeling of Charge-Coupled Device Characteristics," BSTJ, Vol. 51, No. 3, March 1972.
- 11. Electronics, Vol. 45, No. 7, March 27, 1972, p. 29.
- 12. M. F. Thompsett, "A Simple Charge Regenerator for Use with Charge-Transfer Devices etc.," IEEE Jour. Solid State Circuits, Vol. SC-7, No. 3, June 1973, p. 237-242.

Note added in proof:

13. F.L. Schuermeyer, et.al., "New Structures for Charge-Coupled Devices", Proc. of IEEE, Vol.60, No. 11, Nov. 1972, p1444.

(Discussion of P-N and Shottky barrier structures which could be constructed with channel oxide. Applicable to materials other than silicon.)

Trends in Bubble Domain Devices

A review article in IEEE Spectrum¹ brought the subject to the attention of engineers in 1972. A review of the IBM Technical Disclosure Bulletins for 1972 show that there is interest and activity at IBM in bubble applications. Several articles in IEEE Transactions on Magnetics^{2,3,4,5} discussed applications and applications problems for bubble memories, counting circuits and shift registers.

There has been interest in the use of garnets rather than orthoferrites for bubble material because stable bubbles are smaller in garnets. Packing density and speed are higher with the smaller bubbles. A new type of bubble, called a "hard bubble", was observed in garnets. This type of bubble tends to stay elongated, collapses at a higher field and does not move in the direction of the field gradient. Hence it is undesirable. A group of articles^{6,7,8,9} in BSTJ discussed the problem and some cures for it. The gist appears to be that magnetic materials are difficult to understand. The problem is so complex that new phenomena crop up that are unanticipated by seasoned researchers. Again the ingenuity of researchers in the field is evidenced by a multiplicity of solutions to the new problem.

- 1. H. Chang, et. al., "A Self-contained Magnetic Bubble Domain Memory," IEEE Trans. on Mag., Mag-8, No. 2, June 1972, p. 214.
- 2. M. Shoji, "Magnetic Bubble Counting Circuits," (Ibid 1), p. 240.
- 3. J. A. Copeland, "Theory of Single-Current Domain Propagation Circuits," (Ibid) p. 241.
- 4. H. Hayashi, et. al., "An Analysis of a Clear-View Angelfish Bubble-Domain Shift Register," IEEE Trans. on Mag., Mag-8, No. 1, March 1972, p. 16.
- 5. W. J. Tabor, et. al., "A New Type of Cylindrical Magnetic-Domain," BSTJ, Vol. 51, No. 6, July-Aug. 1972, p. 1427.
- 6. A. H. Bobeck, et. al., "Multi-layer Epitaxial Garnet Films for Magnetic-Bubble Device--Hard Bubble Suppression," (Ibid 5), p. 1431.
- 7. R. Wolfe and J. C. North, "Suppression of Hard Bubbles in Magnetic Garnet Films by Ion Implantation," (Ibid 5), p. 1437.
- 8. A. Rosencwaig, "The Effect of a Second Magnetic Layer on Hard Bubbles," (Ibid 5), p. 1440.

Trends in Amorphous Semiconductors

Our survey was limited to the more traditional literature dealing with electronic materials, devices, and circuits. Most of the small amount of material dealt with definitive studies of amorphous materials. We were unable to detect any significant breakthrough with regards to application. The claims of earlier critics that the complex amorphous materials are difficult to prepare in a predictable repeatable way seem to still be valid. One disclosure in the IBM Technical Disclosure Bulletin was of interest in that it proposed the use of laser heating to change the state of an amorphous film thus changing its reflectivity. The method appeared to be impractical in that it required the use of discrete P-N lasers for excitation. However, this is one step in the direction of using amorphous materials for large screen displays which was discussed in our last interim report. This seems to be an area inaccessible to the traditional crystalline semiconductor.

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- 3. Schuocker, Sabalhy, and Langer, "Pulse Response of the Conducting Channel in Thermally Switch Gless Films," Jour. App. Phys., Vol. 43, No. 6, June 1972, p. 2647.
- 4. Arnoldussen, et. al., "Analysis of Photoconductivity in Amorphous Chalcogenides," Jour. App. Phys., Vol. 43, No. 3, March 1972, p. 1112.
- 5. Rockstad, "Amplification in an Amorphous Semiconductor Diode," Jour. App. Phys., Vol. 43, No. 1, Jan. 1972, p. 238.

Trends in Ion Implantation

Publications throughout the year have illustrated the utility of ion implantations for achieving high performance in silicon devices. The applications to CCD's covered in the section on Trends in CCD's are outstanding. Here the problems of interface trapping, complex phasing of the transfer electrodes, and the interelectrode barrier are all attacked using ion implantation. Ion implantation into cadmium sulfide and gallium arsenide were reported. Studies of basic effects produced by ion implantations were also reported.

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- 2. Morehead, et. al., "Formation of Amorphous Silicon by Ion Bombard-ment as Function of Ion, Temperature, and Dose," Ibid 1, p. 1112.
- 3. Shiraki, et. al., "Ion Implantations of Nitrogen into Cadmium Sulfide," Jour, App. Phys., Vol. 43, No. 2, Feb. 1972, p. 710.
- 4. J. F. Gibbons, "Ion Implantations in Semiconductors--Part II: Damage and Annealing," Proc. of IEEE, Vol. 60, No. 9, Sept. 1972, pp. 1062-1097.
- 5. "Ion Implantation Comes of Age," Electronics, Vol. 45, No. 6, May 22, 1972, p. 69.
- 6. "Ion Implants for Low Noise Bipolar Transistors," Electronics, Vol. 45, No. 7, March 1972, p 56.

Trends in Fabrication

Two articles reported the PLANOX 1 and SATO 2 processes which utilize the Si $_3$ N $_4$ (nitride) gate and a thick oxide isolation technique to obtain small dense circuits. A 3-mask bipolar IC structure was reported 3 , and an issue of the IEEE Transactions on Electron Devices 4 was devoted to computer-controlled microfabrication lithographic (photo and E-beam). The field is still very active and all of the new results reported are potentially important ones. One article held forth new hope for the old idea of silicon on sapphire 5 .

- 1. Liectronics, Vol. 44, No. 26, Dec. 20, 1971, pp. 44-48.
- 2. Electronics, Vol. 45, No. 1, Jan. 3, 1972, pp. 89-92.
- 3. IEEE Trans. ED, Vol. ED-19, No. 2, Feb. 1972, p. 182.
- 4. IEEE Trans. Ed, Vol. ED-19, No. 5, May 1972.
- 5. Electronics, Vol. 45, No. 15, Aug. 14, 1972, p. 113.